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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,652	11/26/2003	Kerry Leeds Davison	4-7-23	7648

7590 02/06/2008  
Ryan, Mason & Lewis, LLP  
90 Forest Avenue  
Locust Valley, NY 11560

EXAMINER

NGO, HUNG V

ART UNIT	PAPER NUMBER
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2831

MAIL DATE	DELIVERY MODE
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02/06/2008

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	Application No. 10/722,652	Applicant(s) DAVISON ET AL.	
	Examiner Hung V. Ngo	Art Unit 2831	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-18 and 20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-18 and 20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |  |
|---|--|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                      | 5) <input type="checkbox"/> Notice of Informal Patent Application                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date ____ | 6) <input type="checkbox"/> Other: ____  |

Art Unit: 2831

### DETAILED ACTION

The Board of Patent Appeals and Interferences affirmed the rejection(s) against independent claim(s) 19, but reversed all rejections against claim(s) 1-8, 14, 15, 17, 18, 20. The independent claim(s) 19 is/are cancelled by the examiner in accordance with MPEP § 1214.06.

In view of the new reference found, PROSECUTION IS HEREBY REOPENED.

An office action with a new ground of rejection based on Wu follows:

#### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-18, 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Wu (US 6,770,963).

Re claim 1, Wu discloses an integrated circuit device comprising:

a die (202) having a top surface with a peripheral region (203) and an interior region surrounded by the peripheral region (Fig 2):

a plurality of bond pads (221, 231, 241) disposed in the peripheral region of the die;  
at least one internal bus (204, 206, 208), disposed in the interior region of the die, that

Art Unit: 2831

distributes power to a plurality of internal node points of the die; and

at least one bond wire connecting at least one of the plurality of bond pads with the at least one internal bus (Fig 2).

Re claim 2, wherein the at least one internal bus comprises a metal power grid (col. 9, lines 35-40).

Re claim 3, wherein the at least one internal bus comprises at least one internal positive voltage supply bus (col. 9, lines 35-40).

Re claim 4. The integrated circuit device of claim 1, wherein the at least one internal bus comprises at least one internal negative voltage supply bus (col. 8, lines 15-20)(abstract).

Re claim 5, wherein the at least one internal bus comprises at least one pair of buses comprising an internal positive voltage supply bus and internal negative voltage supply bus (col. 9, lines 35-40), (col. 8, lines 15-20).

Re claim 6, wherein at least one of the voltage supply buses comprises a ground bus (col. 8, lines 15-20) (abstract).

Re claim 7, wherein the at least one internal bus comprises bond pads having active circuitry (integrated circuit in the die 202) disposed thereunder.

Re claim 8, wherein at least one of the plurality of bond pads is wire bonded to an integrated circuit package (100),(Fig 2).

Re claim 9, wherein the at least one of the plurality of bond pads wire bonded to the at least one internal bus is also wire bonded via another bond wire to a positive voltage supply terminal (106) of the device.

Art Unit: 2831

Re claim 10, wherein, the positive voltage supply terminal comprises a positive voltage supply ring surrounding the die (Fig 2)

Re claim 11, wherein the at least one of the plurality of bond pads wire bonded to the at least one internal bus is also wire bonded via another bond wire to a negative voltage supply terminal (106) of the device (Fig 2).

Re claim 12, wherein, the negative voltage supply terminal comprises a negative voltage supply ring surrounding the die (Fig 2)

Re claim 13, wherein the at least one of the plurality of bond pads wire bonded to the at least one internal bus is connected to another of the plurality of bond pads (Fig 2).

Re claim 14, further comprising local power interconnects that distribute power from the at least one internal bus to the plurality of internal node points (Fig 2).

Re claim 15, wherein the plurality of internal node points comprise circuit elements (Fig 2).

Re claim 16, wherein the power is distributed from the at least one of the plurality of bond pads to at least one secondary bond pad (106) through a metal connector (114, 116), and from the at least one secondary bond pad to the at least one internal bus through at least one wire bond connection within the peripheral region of the die (Fig 2).

Re claim 17, wherein the at least one of the plurality of bond pads comprises at least one pair of bond pads comprising a positive voltage supply bond pad and a negative voltage supply bond pad (abstract).

Re claim 18, wherein the at least one pair of bond pads comprises at least about twelve pairs of bond pads substantially evenly spaced apart in the peripheral region of the die

Art Unit: 2831

(Fig 2).

Re claim 20, Wu disclose a method of constructing an integrated circuit device comprising the following steps: forming an integrated circuit die (202) having at least one peripheral bond pad (221, 231, 241) and at least one internal bus (204, 206, 208), the internal bus being configured for distributing power to a plurality of internal node points of the integrated circuit device (Fig 2); and wire bonding the at least one peripheral bond pad to the at least one internal bus (Fig 2).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung V. Ngo whose telephone number is (571) 272-1979. The examiner can normally be reached on Monday to Thursday 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego Gutierrez can be reached on (571) 272-2800 EXT 31. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2831

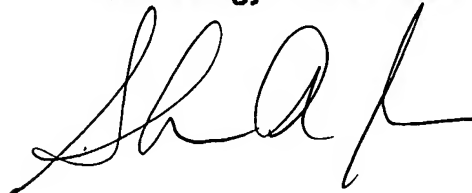
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/Hung V Ngo/

Primary Examiner, Art Unit 2831

01/29/08

**Sharon A. Gibson**  
Director  
Technology Center 2800

A handwritten signature in black ink, appearing to read 'Sharon A. Gibson', written over the printed name and title.